The opinion in support of the decision being entered today was *not* written
for publication and is *not* binding precedent of the Board.
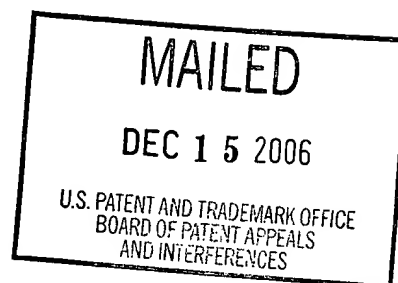
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PETRA LEBER, JENS LEENSTRA,
WOLFRAM SAUER, and DIETER WENDEL

Appeal No. 2006-3138
Application No. 09/683,351
Technology Center 2100

ON BRIEF

MAILED

DEC 1 5 2006

U.S. PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS
AND INTERFERENCES

Before THOMAS, RUGGIERO, and DIXON, *Administrative Patent Judges.*

DIXON, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the Examiner's final
rejection of claims 1-10, which are all of the claims pending in this application.
Appellants have elected not to appeal the rejection of claim 6 under 35 U.S.C. § 103.

We REVERSE.

BACKGROUND

Appellants' invention relates to a method for handling 32-bit results for an out-of-order processor with a 64-bit architecture. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

> 1. A method for operating a processor having an architecture of a larger bit-length with a program comprising instructions compiled to produce instruction results of at least one smaller bit-length, characterized by the steps of:
>
> detecting when in program order a first instruction is to be dispatched which does not have a target register address as one of its sources, wherein the first instruction is one of the instructions compiled to produce instruction results of at least one smaller bit-length;
>
> adding an extract instruction into an instruction stream before the first instruction, the extract instruction comprising the following steps of:
>
> a. dispatching the extract instruction together with the following first instruction from an instruction queue into a Reservation Station;
>
> b. issuing the extract instruction to an Instructional Execution Unit (IEU) as soon as all source operand data is available and an IEU is available according to respective issue scheme;
>
> c. executing the extract instruction by an available IEU;
>
> d. setting an indication that the result of said extract instruction needs to be written into a result field of the first instruction following the extract instruction, and;
>
> e. writing the extract instruction result into the result field of said first instruction, and into all fields of operands being dependent of said first instruction.

PRIOR ART

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Mahurin et al. (Mahurin)	6,493,819	Dec. 10, 2002
Isaman et al. (Isaman)	6,449,710	Sep. 10, 2002

Johnson, Mike; (Johnson) "Superscalar Microprocessor Design," Prentice-Hall, Inc., pp. 133-134 (1991).

Hennessy, John L. and Patterson, David A. (Hennessy), "Computer Organization and Design, The Hardware/Software Interface," Morgan Kaufmann Publishers, Inc., pp. 118-119, 175, 185, 384, B-9 and the back inside cover (1998).

REJECTIONS

Rather than reiterate the conflicting viewpoints advanced by the Examiner and the Appellants regarding the above-noted rejections, we make reference to the Examiner's answer (mailed Feb. 24, 2006) for the reasoning in support of the rejection, and to Appellants' brief (filed Nov. 16, 2005) for the arguments thereagainst.

The Examiner has withdrawn the rejection of claims 1-10 under 35 U.S.C. § 112, Second Paragraph. Claims 1-5 and 7-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Mahurin in view of Isaman, Johnson, and Hennessy.

OPINION

In reaching our decision in this appeal, we have given careful consideration to Appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by Appellants and the Examiner. As a consequence of our review, we make the determinations that follow.

35 U.S.C. § 103

In rejecting claims under 35 U.S.C. § 103, the examiner bears the initial burden of presenting a prima facie case of obviousness. See In re Rijckaert, 9 F.3d 1531, 1532, 28 USPQ2d 1955, 1956 (Fed. Cir. 1993). A prima facie case of obviousness is established by presenting evidence that the reference teachings would appear to be sufficient for one of ordinary skill in the relevant art having the references before him to make the proposed combination or other modification. See In re Lintner, 458 F.2d 1013, 1016, 173 USPQ 560, 562 (CCPA 1972). Furthermore, the conclusion that the claimed subject matter is prima facie obvious must be supported by evidence, as shown by some

objective teaching in the prior art or by knowledge generally available to one of ordinary skill in the art that would have led that individual to combine the relevant teachings of the references to arrive at the claimed invention. See In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Rejections based on § 103 must rest on a factual basis with these facts being interpreted without hindsight reconstruction of the invention from the prior art. The examiner may not, because of doubt that the invention is patentable, resort to speculation, unfounded assumption or hindsight reconstruction to supply deficiencies in the factual basis for the rejection. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 177 (CCPA 1967). Our reviewing court has repeatedly cautioned against employing hindsight by using the appellant's disclosure as a blueprint to reconstruct the claimed invention from the isolated teachings of the prior art. See, e.g., Grain Processing Corp. v. American Maize-Prods. Co., 840 F.2d 902, 907, 5 USPQ2d 1788, 1792 (Fed. Cir. 1988).

When determining obviousness, "the [E]xaminer can satisfy the burden of showing obviousness of the combination 'only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references.'" In re Lee, 277 F.3d 1338, 1343, 61 USPQ2d 1430, 1434 (Fed. Cir. 2002), citing In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). "Broad conclusory statements regarding the teaching of multiple references, standing alone, are not 'evidence.'" In re Dembiczak, 175 F.3d 994, 999, 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). "Mere denials and conclusory statements, however, are not sufficient to establish a genuine issue of material fact." Dembiczak, 175 F.3d at 999-1000, 50 USPQ2d at 1617, citing McElmurry v. Arkansas Power & Light Co., 995 F.2d 1576, 1578, 27 USPQ2d 1129, 1131 (Fed. Cir. 1993).

Further, as pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." In re Hiniker Co., 150 F.3d 1362,1369, 47 USPQ2d 1523, 1529 (Fed. Cir. 1998). Therefore, we look to the limitations as recited in independent claim 1. Here, the Examiner has relied basically on the teachings of Mahurin. (Answer, pp. 5-14). From our review of the Examiner's statement of the rejection and of the responsive arguments (Answer, pp. 17-38), we cannot agree with the Examiner's finding concerning the combination of the references and the suggestion in Isaman to use a separate read instruction for the read operation of Mahurin.

Furthermore, we find that the Examiner maintains in the statement of the present rejection that Mahurin teaches a read "operation" (the Final rejection just used the term "read" without operation or instruction), the Final rejection also states that "a hardware reduction can occur" (Final Rejection, p. 8, l. 6) and "[t]he hardware could then be simplified and reduced in the reservation station" (Final Rejection, p. 8, ll. 13-14).

Appellant argues:

> Throughout all of his rejections, the Examiner makes the flawed assumption that in Mahurin, the "read operation" is an "instruction" executed by the functional units 24 of Figure 1. That is, when Mahurin refers to "instructions," the Examiner assumes that this necessarily includes the "read operation." At no point does Mahurin refer to the "read operation" as an "instruction." At no point does Mahurin even state the function units 24 perform the "read operation." Indeed, that Mahurin does not refer to the "read operation" as an "instruction" strongly indicates that Mahurin intends for the "read operation" to not be an "instruction." Therefore, the Examiner cannot simply interpret the "read operation" as an "instruction" in hindsight. Such an interpretation is clearly improper. (Br. 11, ll. 12-20).

We agree with Appellants that the Examiner seems to make the leap from the read operation of Mahurin to the combination with Isaman which teaches separate instructions to then detect and insert an extract instruction before the detected instruction.

We find that the Examiner is relying upon improper hindsight to reconstruct the claimed invention. We find no teaching or suggestion in Mahurin or Isaman to make the proposed combination as advanced by the Examiner. We find that the main point of contention is that the read "operation" of Mahurin is an operation rather than an instruction. We find that the Examiner discusses the teachings of Mahurin initially as an "operation" and later states that Mahurin teaches a read "instruction" in the responsive arguments:

> xiii. The reduction and simplification of hardware would have provided motivation to implement the read instruction of Mahurin in a separate microinstruction inserted into the instruction stream by the MROM unit 34." Final Office Action (6/8/05) **(Emphasis added by Examiner to indicate a specific example of an objective teaching in the prior art that was used as motivation for the combination)**. [Answer, p. 31].

We find the Examiner's rejection replete with statements such as, "can," "could," and "would require." While the Examiner may have a strong contention that the claimed invention would have been obvious to one of ordinary skill in the relevant art at the time of the invention, the Examiner bears the initial burden of persuasion for presenting a prima facie case of obviousness. Here, we cannot find that the Examiner has set forth a sufficiently clear case supported by a convincing line of reasoning for the analysis and combination. Therefore, we cannot find that the Examiner has met the initial burden.
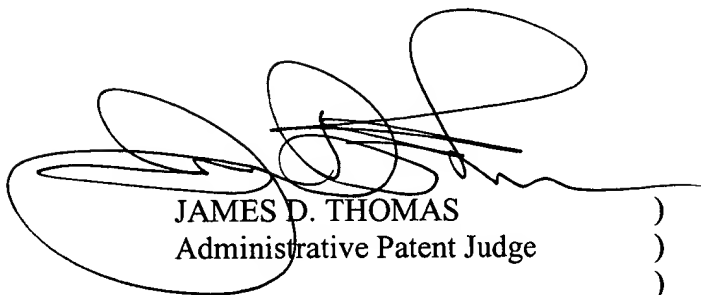
While we agree with the Examiner that Mahurin teaches the use of a read operation and Isaman the use of inserting microinstructions, we cannot make the leap that it would have been obvious to one of ordinary skill in the relevant art at the time of the invention to identify a specific instruction which is disclosed as an operation and to then combine it with a teaching of an instruction and insertion of a read instruction as the Examiner seems to over simplify. While each individual step or modification that the Examiner makes to the base teachings of Mahurin may seem to be not too great a leap, we cannot agree with the totality of the Examiner's modifications, analysis and combination. Therefore, we cannot find that the Examiner has established a prima facie case of obviousness of the invention as recited in independent claim 1 and dependent claims 2-5 and 7.

Similarly, we cannot sustain the rejection of independent claims 8, 9, and 10 since we cannot find that the Examiner has established a sufficiently clear case of obviousness of the invention recited in these claims.
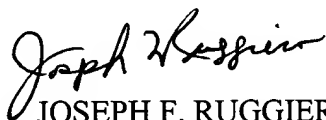
CONCLUSION

To summarize, we have reversed the Examiner's rejection of claims 1-5 and 7-10 under 35 U.S.C. § 103.

REVERSED

JAMES D. THOMAS
Administrative Patent Judge
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) BOARD OF PATENT
JOSEPH F. RUGGIERO) APPEALS
Administrative Patent Judge) AND
) INTERFERENCES
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JOSEPH L. DIXON)
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